A COMPARATIVE STUDY OF SEPIC, CUK AND ZETA CONVERTERS

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Abstract: ***In this paper a comparative study of DC-DC converters is presented. The SEPIC, Cuk and ZETA converters in applications are detailed. Also are presented the operating simulation for these converters. The results of simulations are compared with the measurements done for a ZETA converter with an output of 3.3V and different output currents.***

Keywords: ***DC-DC converters, SEPIC converter, Cuk converter, ZETA converter***

1. INTRODUCTION

It's well known that to have the maximum efficiency of the solar panels, the load must be connected to the solar panel through a DC-DC converter. The topologies and the operation of these converters are very well described in the literature. A classification of these converters is presented in [1]. The authors of [1] consider the DC-DC converters in six decades: (1) classical/traditional converters, (2) multiple-quadrant converters, (3) switched component converters, (4) soft-switching converters, (5) synchronous rectifier converters, (6) multiple energy-storage elements resonant converters. The classical/traditional converters are divided in five categories: (1) fundamental converters, (2) transformer-type converters, (3) developed converters, (4) voltage-lift converters, and (5) super-lift converters.

The converters studied in this paper are classical developed converters well known in literature like converters in SEPIC (Single Ended Primary Inductance Converter) topology, Cuk and ZETA (Positive Output Luo Converter). The developed-type converters derived from fundamental converters by addition of a low-pass filter. In [2] these converters are considered like a MASTER converter switched by a PWM signal, and a SLAVE converter achieved with passive components.

Because the great usage of converters in the topologies mentioned above in applications, we found opportunity for a short presentation of operating principles, simulations and some experimental results in this work. The equations of main operating parameters, advantages and disadvantages of each topology are presented in chapter 2 of this paper. The simulations and the measurements are presented in chapter 3, and the final conclusions in chapter 4.

2.1. OPERATING PRINCIPLES

2.1 Fundamental DC-DC Converters

From the viewpoint of input and output voltages – V_1 and V_o, the fundamental converters are: (1) step-down or buck converters, (2) step-up or boost converters, (3) step down/up or buck-boost converters. Figure 1 shows the principle diagrams of these topologies.

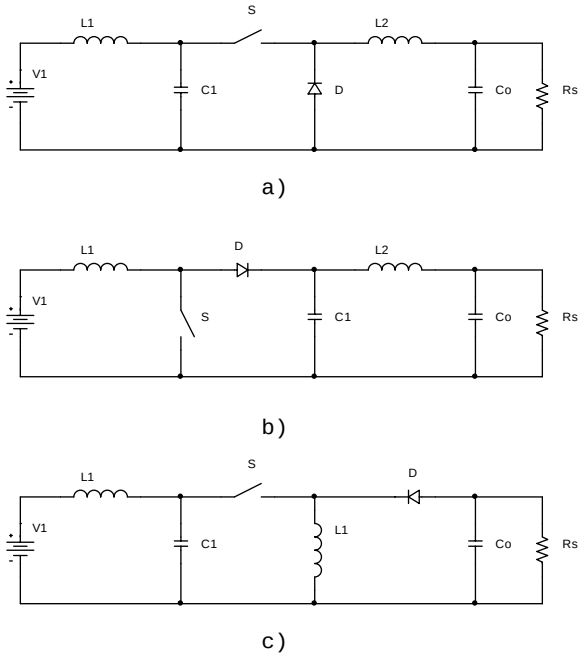

Figure 1. Fundamental DC-DC Converters: a) buck converter, b) boost converter, c) buck-boost converter.

In ideal operating conditions (no voltage loss on the switch S, the average voltage across inductors L at steady state zero, no current loss on capacitors C, and no voltage loss on diode at forward conduction) the equations of ratio V_o/V_1 are:

– for the buck converter (1):

$$\frac{V_o}{V_1} = D \qquad (1)$$

where D is the duty cycle of PWM signal of switch S, with the meaning from equation (2),

$$D = \frac{t_{ON}}{T} \qquad (2)$$

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where t_{ON} is the conduction time of switch S and T is the period of PWM signal.

– for the boost converter (3):

$$\frac{V_o}{V_1} = \frac{1}{1-D} \tag{3}$$

– for the buck-boost converter (4):

$$\frac{V_o}{V_1} = \frac{D}{1-D} \tag{4}$$

In all these equations the internal resistance of power supply V_1 was considered zero [3].

2.2. Developed DC-DC converters

Figure 2 shows the topologies of developed DC-DC converters.

These topologies have few similitudes:

– The equation of the transfer function of these converters is (4), the same with that one of buck-boost converter, if the conditions of Continuous Conduction Mode – CCM are assured.

– These converters are used in different applications, such as with solar panels, in systems supplied with electrical energy where the output voltage V_o of converter can be superior or inferior of the input voltage V_1 of converter. The fundamental converters don't accept this situation. These converters are integrated in the MPPT of solar panels.

– The capacitor C assures the galvanic insulation between input and output. The short-circuits or others breakdown of the load don't affect the power supply – solar panels.

– The output voltage becomes zero if the PWM control signal of switch S is missing.

– The diode D can be replaced by a transistor switched synchronal with the main switch in the synchronous converters.

The differences between these topologies are:

– SEPIC and Cuk converters became from the boost converter, and ZETA converter from the buck-boost converter.

– The ripple current in the load is greater for Cuk and ZETA converters than SEPIC, because the SEPIC converter has an inductor L_2 that smooth the current spikes.

– The switch S of SEPIC ad Cuk converters is a N channel MOS transistor that needs a Low Side driver, when the ZETA converter has a P channel MOS transistor that needs a High Side driver.

Because, these three topologies have many advantages mentioned above, these things make enable their integration in applications with a great efficiency of using the solar energy in solar panels with MPP trackers.

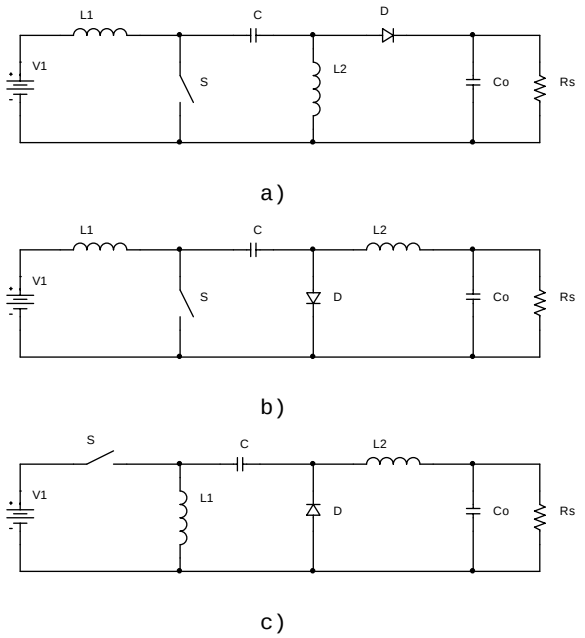


Figure 2. Developed DC-DC Converters: a) SEPIC converter, b) Cuk converter, c) ZETA converter

2.3 Integration of convertors in MPPT systems

The perturb-and–observe (PAO) method for the MPPT is an iterative approach. The MPP is obtained by making the derivate of power equal with zero in the feedback circuit that commands the duty cycle of switch S. This is very useful because doesn't need the disconnection of panels from the load. Through this method can be reached good results if it is compared the instantaneous conductance of panel with the incremental conductance of panel – the method is known as Incremental Conductance Technique (ICT) [4].

If it is considered the equivalent circuit of the solar panel like in Fig. 3, with v_i the input voltage of panel and r_i the equivalent input resistance of panel, P_i the input power, P_o the output power (5), the $\partial P = 0$ means (6).

$$P_i = P_o = \frac{v_i^2}{r_i} \tag{5}$$

$$\frac{\partial v_i}{\partial r_i} = \frac{V_i}{2R_i} \tag{6}$$

The method proposed in [4] resides in the connection of a SEPIC or Cuk converter between the solar panel and load. The converter works in continuous current mode (CCM) through inductor L_1 – Figure 2 a), but with discontinuous voltage (DCV) on the capacitor C. The duty cycle of PWM signal of switch is adjusted in a proper way to achieve the input resistance of converter equal with the output resistance of solar panel. Figure 3 shows the equivalent circuit of solar panel and converter.

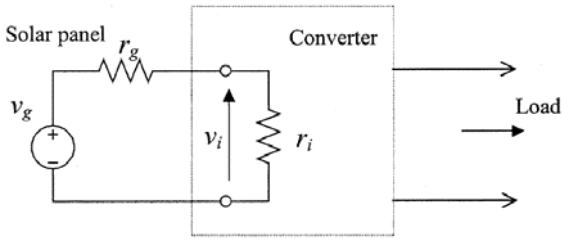


Figure 3. Equivalent circuit of a solar panel and converter [4]

The operating equations of SEPIC converter in DCV mode are the next: (7a) – the voltage on capacitor C, (7b) – the voltage on diode D.

$$v_C(t)=\begin{cases}\dfrac{I_1(1-d)T_S}{C}-V_o-\dfrac{I_2}{C}t, 0<t<d_1T_S\\ -V_o, \qquad d_1T_S<t<dT_S\\ \dfrac{I_1}{C}(t-dT_S)-V_o, \qquad dT_S<t<T_S\end{cases} \quad (7a)$$

$$v_D(t)=\begin{cases}V_o+v_C(t), 0<t<d_1T_S\\ 0, \qquad d_1T_S<t<T_S\end{cases} \quad (7b)$$

where I_1 and I_2 are the inductor currents - assumed to be constant, dT_S is the conduction time of switch, d_1T_S is the conduction time of diode D, and T_S is the period of PWM signal of switch - $T_S=\dfrac{1}{f_S}$, f_S – frequency of PWM signal.

The three sequences in one switching cycle are shown in Figure 4.

Because the voltage of capacitor C at d_1T_S is $v_C(d_1T_S)=-V_o$, the duty cycle is $d_1=\dfrac{I_1}{I_2}(1-d)$.

In the steady state the voltage on the inductor L_2 is zero. From this moment the output voltage V_o is equal with the average voltage of diode D (8).

$$V_o=\frac{1}{T_S}\int_0^{d_1T_S}v_D(t)dt=\frac{T_S}{2C}I_1(1-d)d_1 \quad (8)$$

Moreover, the voltage stress on the switch S is given by (9).

In the same way can be determined the operating equations of Cuk and ZETA topologies. This is shown in [4].

$$v_{stres}=v_C(T_S)+V_o=\frac{I_1}{C}(1-d)T_S \quad (9)$$

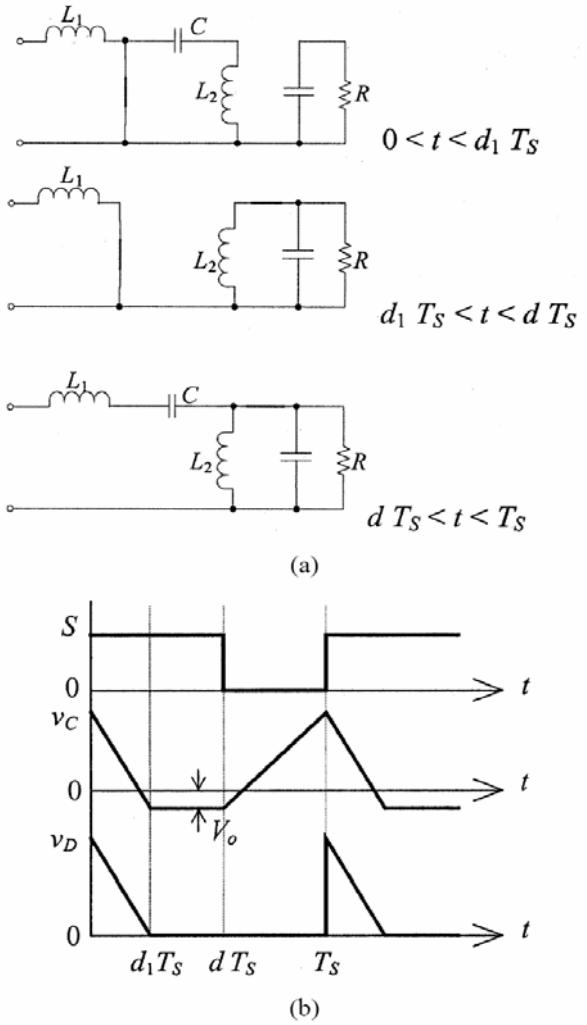


Figure 4. Operating principle of the SEPIC converter. a) equivalent circuits, b) theoretical waveforms [4]

3. Simulations

In this chapter it will be presented few representative waveforms of each topology. The simulations were done in OrCAD, in the next conditions:

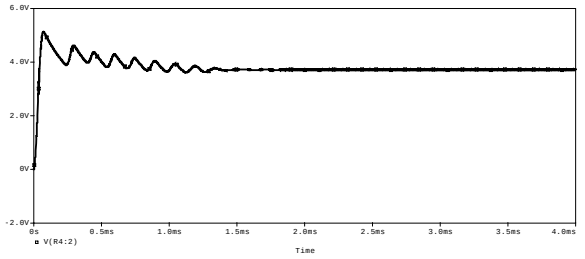
- input voltage – V_1=12V,
- output voltage – V_o=3.3V,
- load resistance – R_S=3.3Ω,
- duty cycle – D=0.22,
- switching frequency – f_S=500kHz,
- coupling capacitor C=47μF,
- output capacitor C_o=100μF,
- inductors L_1=L_2=6.2μH.

3.1 The SEPIC converter

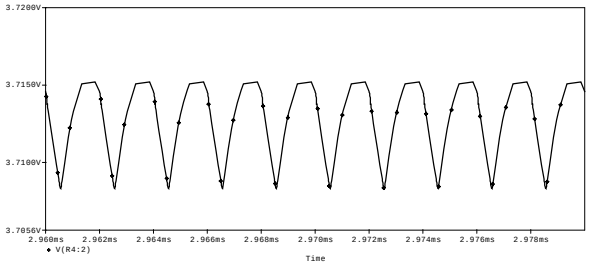
To simulate the operation of SEPIC converters it was used the diagram from Figure 2 a). In Figure 5 a), b), and c), is shown the output voltage V_o, the ripple of

output voltage ΔV_o, and the voltage stress V_{stress} of switch S.

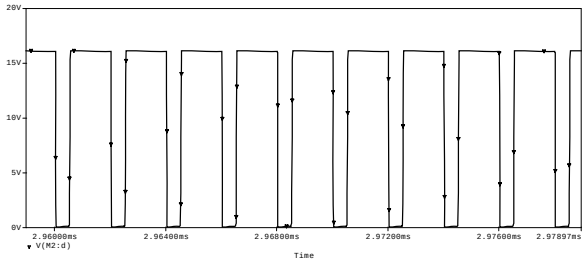
At steady state – after 1.5ms, these values are: V_0=3.5V, ΔV_o=6mV_{pp}, and V_{stress}=16V.



a) V_o – output voltage



b) ΔV_o – output ripple



c) V_{stress} – voltage stress on switch

Figure 5. Simulated waveforms of SEPIC converter: a) output voltage, b) output ripple, c) voltage stress of switch

3.2. The Cuk conveter

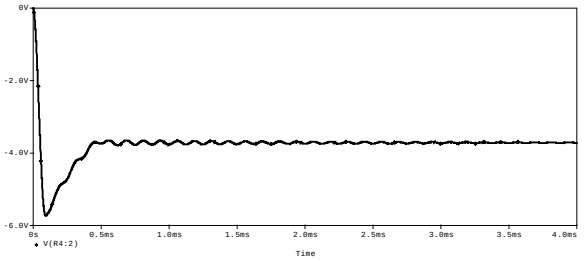
To simulate the operation of Cuk converter it was used the diagram from Figure 2 b). Figure 6 a), b) and c) shows the waveforms of output voltage, output ripple and voltage stress of switch in the same conditions.

At steady state – after 0.5ms, these values are: V_0=3.51V, ΔV_o=28mV_{pp}, and V_{stress}=16V.

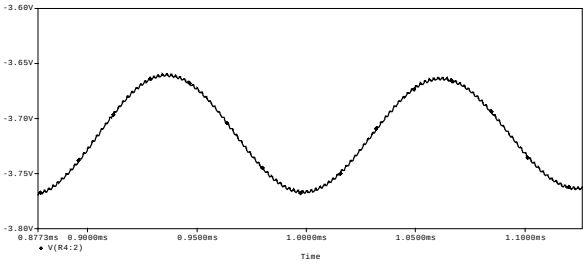
3.3. The ZETA converter

To simulate the operation of ZETA converter it was used the diagram from Figure 2 c). Figure 7 a), b) and c) shows the waveforms of output voltage, output ripple and voltage stress of switch in the same conditions.

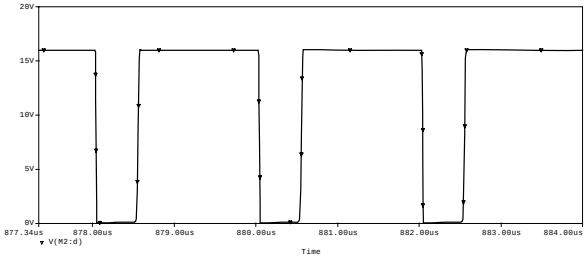
At steady state – after 0.5ms, these values are: V_0=3.41V, ΔV_o=26mV_{pp}, and V_{stress}=16V.



a) V_o – output voltage



b) ΔV_o – output ripple



c) V_{stress} – voltage stress on switch

Figure 6. Simulated waveforms of Cuk converter: a) output voltage, b) output ripple, c) voltage stress of switch

Conclusions on simulations are in Table 1.

Table 1. Simulation Results

Voltage	Topology		
	SEPIC	**Cuk**	**ZETA**
V_o [V]	3.51	3.51	3.41
ΔV_o [mV_{pp}]	6	28	26
V_{stress} [V]	16	16	16

3.4. Experimental verifications

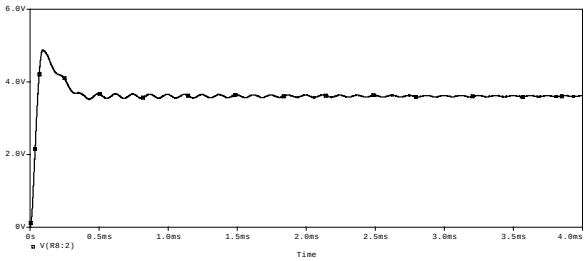
An experiment has been performed using a ZETA topology on a LTC1622 – a Current Mode Step-Down DC/DC converter of Linear Technology [5]. The schematic diagram is the typical application proposed by the producer and is shown in Figure 8 [6].

In Figure 9 are the waveforms in the next conditions: V_I=8.3V, V_o=3.3V, R_S=20Ω (I_o=165mA).

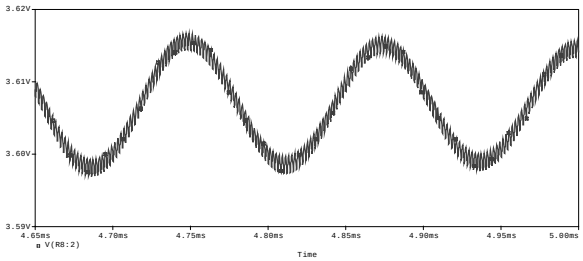
The channels of oscilloscope represent: CH1 – V_G – PWM signal on the gate of MOS transistor, CH2 – V_D – drain voltage of MOS transistor, CH3 – V_C – voltage

on positive pin of capacitor C, CH4 – ΔV_o – output voltage ripple.

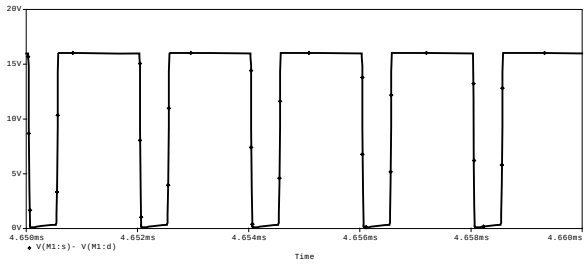
In Figure 10 are the waveforms in these conditions: V_1=4.9V, V_o=3.4V, R_S=10Ω (I_o=340mA). It can be observed other values for switching frequency and duty cycle of PWM signal.



a) V_o – output voltage



b) ΔV_o – output ripple



c) V_{stress} – voltage stress on switch

Figure 7. Simulated waveforms of ZETA converter: a) output voltage, b) output ripple, c) voltage stress of switch

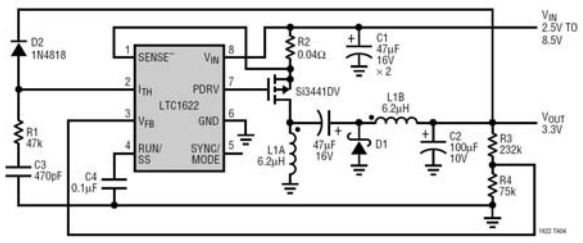


Figure 8. ZETA converter with LTC1622 [9]

The experimental waveforms in the conditions: V_1=7.1V, V_o=3.4V, R_S=5Ω (I_o=680mA) are shown in Figure 11.

It can be seen that the ZETA converter build with the LTC1622 integrated circuit works well with input voltages less than output voltage and at an input voltage over the output voltage. This advantage can be used in systems where these conditions are reached very often – like solar panels in different levels of solar radiation. The results of measurements are in Table 2.

The circuit LTC1622 changes the switching frequency – Figure 9, 10, 11, in a wide range – from 265 kHz to 1024 kHz. Also, the duty cycle D of PWM signal in the gate of the MOS transistor is changed according with the work conditions – input and output voltage, and the output current, to insure a constant value of output voltage.

The ripple of output voltage measured in real conditions is few times greater than that one obtained in ideal conditions of simulations.

Figure 9. Waveforms of V_G, V_D, V_C, ΔV_o in conditions: V_1=8.3V, V_o=3.3V, R_S=20Ω

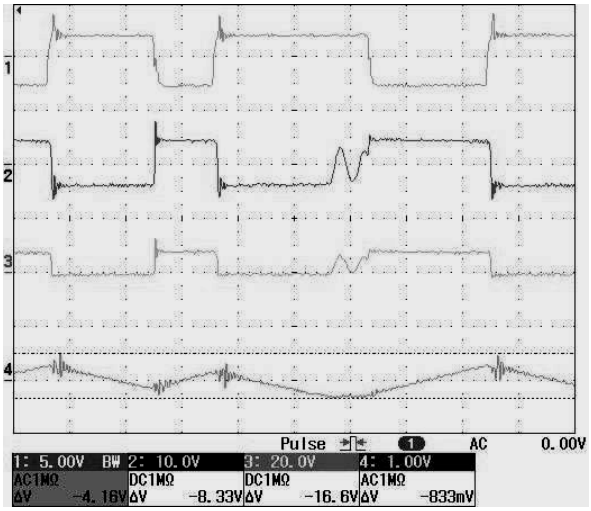


Figure 10. Waveforms of V_G, V_D, V_C, ΔV_o in conditions: V_1=4.9V, V_o=3.4V, R_S=10Ω

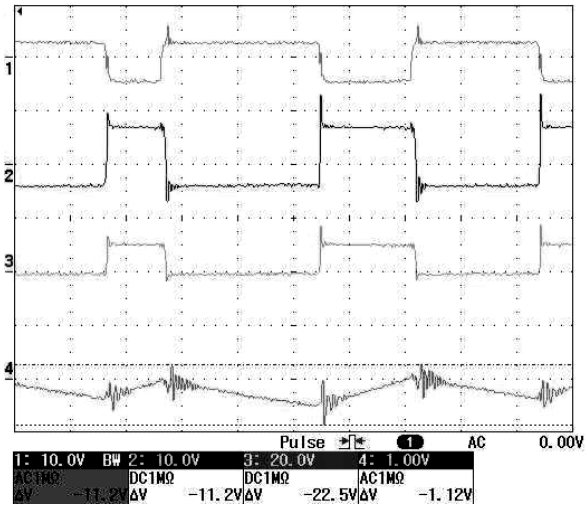


Figure 11. Waveforms of V_G, V_D, V_C, ΔV_o in conditions: V_1=7,1V, V_o=3,4V, R_S=5Ω

Table 2. Measurement results

Voltage	**ZETA converter with LTC1622 with output voltage 3.3V**			
	V_1=8.3V, I_o=165mA	V_1=4.8V, I_o=165mA	V_1=3.2V, I_o=165mA	
ΔV_o [V_{pp}]	1.37	0.82	0.60	
f_S [kHz]	265	524	504	
Voltage	V_1=8.3V, I_o=340mA	V_1=4.9V, I_o=340mA	V_1=8.3V, I_o=680mA	V_1=7.1V, I_o=680mA
ΔV_o [V_{pp}]	1.25	0.83	1.45	1.12
f_S [kHz]	913	759	1024	562

4. CONCLUSIONS

In this paper was presented a comparative study of DC-DC converters in SEPIC, Cuk and ZETA topologies.

It was studied the fundamental converters and developed converters in the topologies mentioned above. The operation equations of main parameters were presented.

Moreover, it was presented the simulations of these converters in the same work conditions.

The waveforms that have seen on a ZETA converter with a constant output voltage and variable input voltage and load confirmed the simulations results of that converter.

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